AI-Driven Multi-Parameters Multi-Objectives Automatic Optimization For Transmission Line In High-Speed SerDes IP

Long Qin[1,2], JinRong Yan[1,2], Hang Sun[1,2], Xuewei Ding[1,2], Xiaomei You[3], Rodger Luo[3], Jie Cheng[3]
(1.State Key Laboratory of Mobile Network and Mobile Multimedia Technology
2.Sanechips Technology Co.,Ltd
3.Ansys Inc)

62 THE CHIPS TO SYSTEMS CONFERENCE

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Motivation

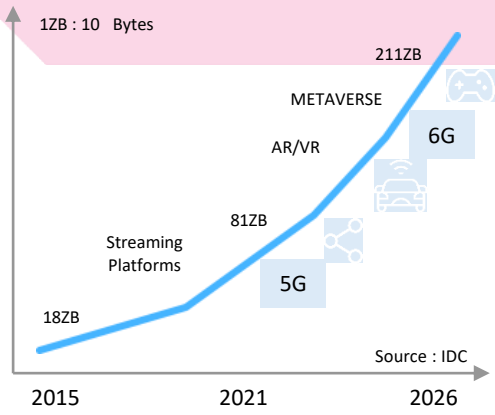
Technology Trends

- The importance of IP in advanced node chips is rising with the growth of the HPC market.
- Data traffic continues to surge across AI, cloud, and data center applications.
- Interface IPs are becoming more complex, requiring higher speed, bandwidth, and performance.

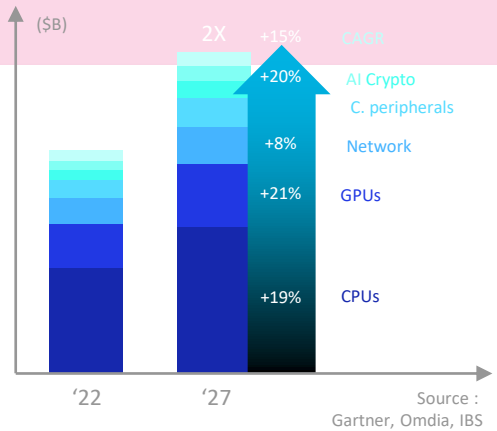
High-Speed SerDes IP Design Challenge

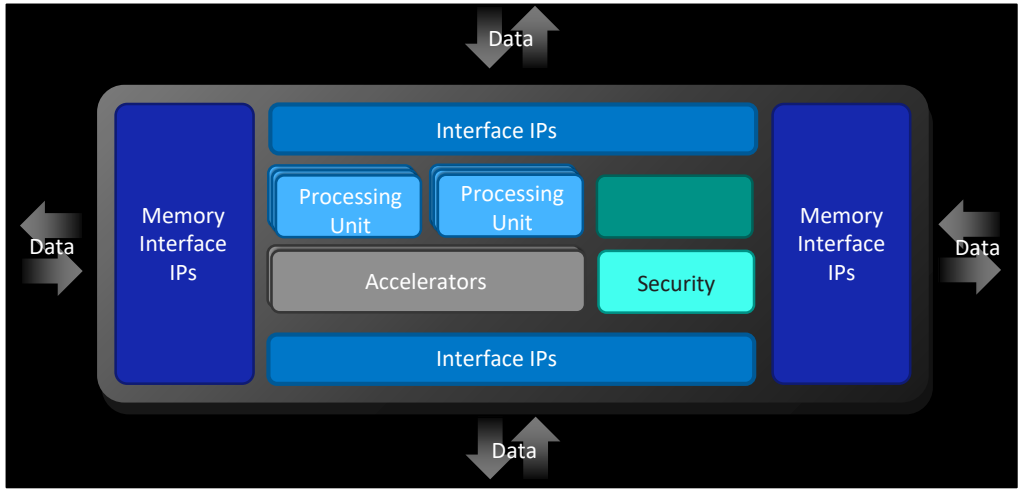
- Signal integrity becomes critical as SerDes data rates and trace lengths increase.
- Transmission line behavior is highly sensitive to layout parameters in advanced nodes.
- Accurate and efficient modeling is essential for reliable and optimized high-speed design.

Global Data Traffic Forecast



HPC Market Forecasts





Limitations of Traditional Design

In modern SerDes IPs, transmission lines are essential for high-speed performance. Traditionally, clock distribution structures are modeled using lumped-RC models. However, as chips become larger and operating frequencies increase, EM-aware transmission line modeling becomes necessary—introducing new design challenges.

Time-consuming EM Simulation

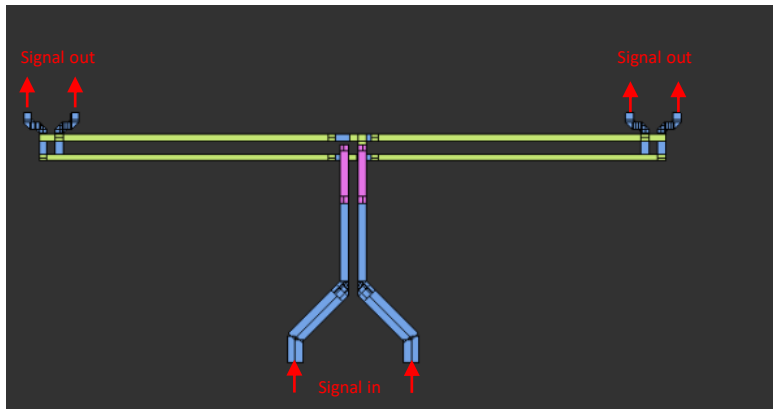
- Accurate RLCk extraction requires lengthy full-wave simulations.

Complex Parameter Optimization

- Designers must tune many variables (width, spacing, thickness, length, layer, shielding, etc.) under tight constraints.

Long Iteration Cycles

- Integrating extracted S-parameters into the testbench, evaluating performance metrics, adjusting the layout, and re-running extraction and simulation is a time-consuming and repetitive process.

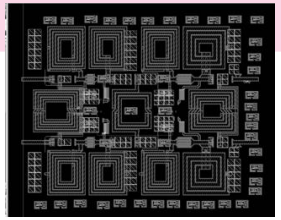


For example: Differential transmission lines in high-speed SerDes IP

- Process: Advanced node
- Frequency: ≥50G
- Transmit two sets of different high-speed differential signals
- Complex routing environment

An **AI-driven, EM-aware automatic optimization framework** is urgently needed to address these challenges efficiently and accurately.

Proposed AI-Driven Optimization Flow



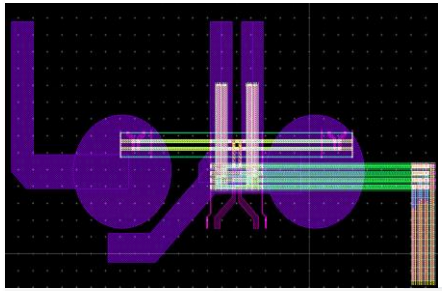
Best transmission line routing for optimum **circuit performance**?

Multi-Parameters

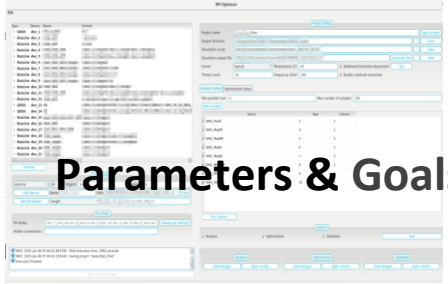
Multi-Objectives

SerDes/RF IC Designer

Parametrization



Initial layout



Parameters & Goals

Layout Modeling & Simulation

optiSLang Metamodel

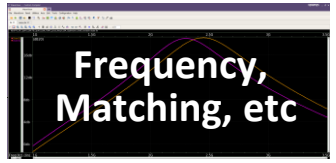
Electromagnetic modeling

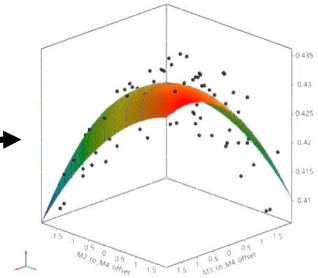
RaptorX
EM engine

Circuit Simulation

Circuit
Analysis

Metrics Calculation





/HFSS IC Pro AI

Metamodel Training

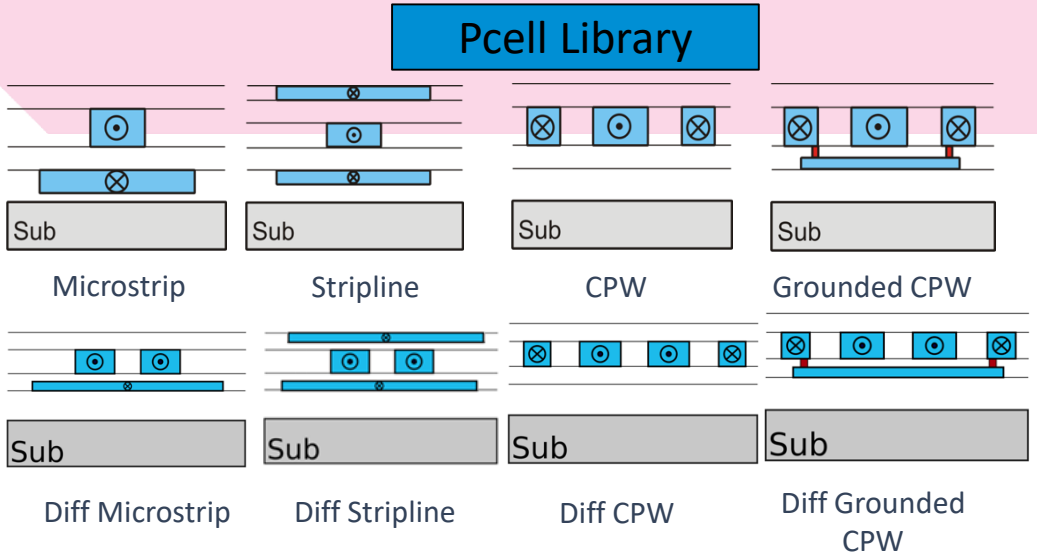
~~WEEKS~~ → DAYS

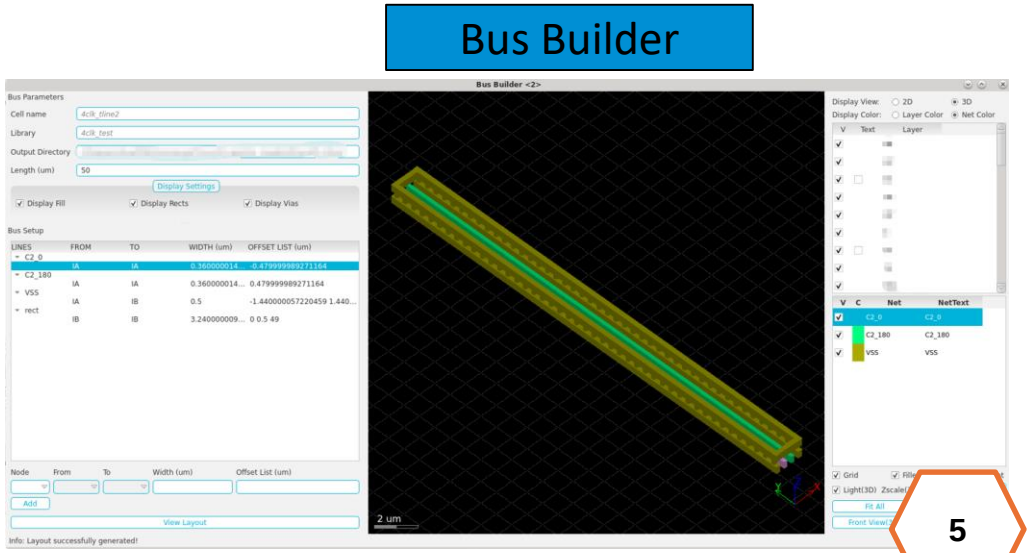
~~DAYS~~ → HOURS

With the power of AI, go from a "good enough" to an optimal layout, while reducing iteration time!

Benefits of This Flow

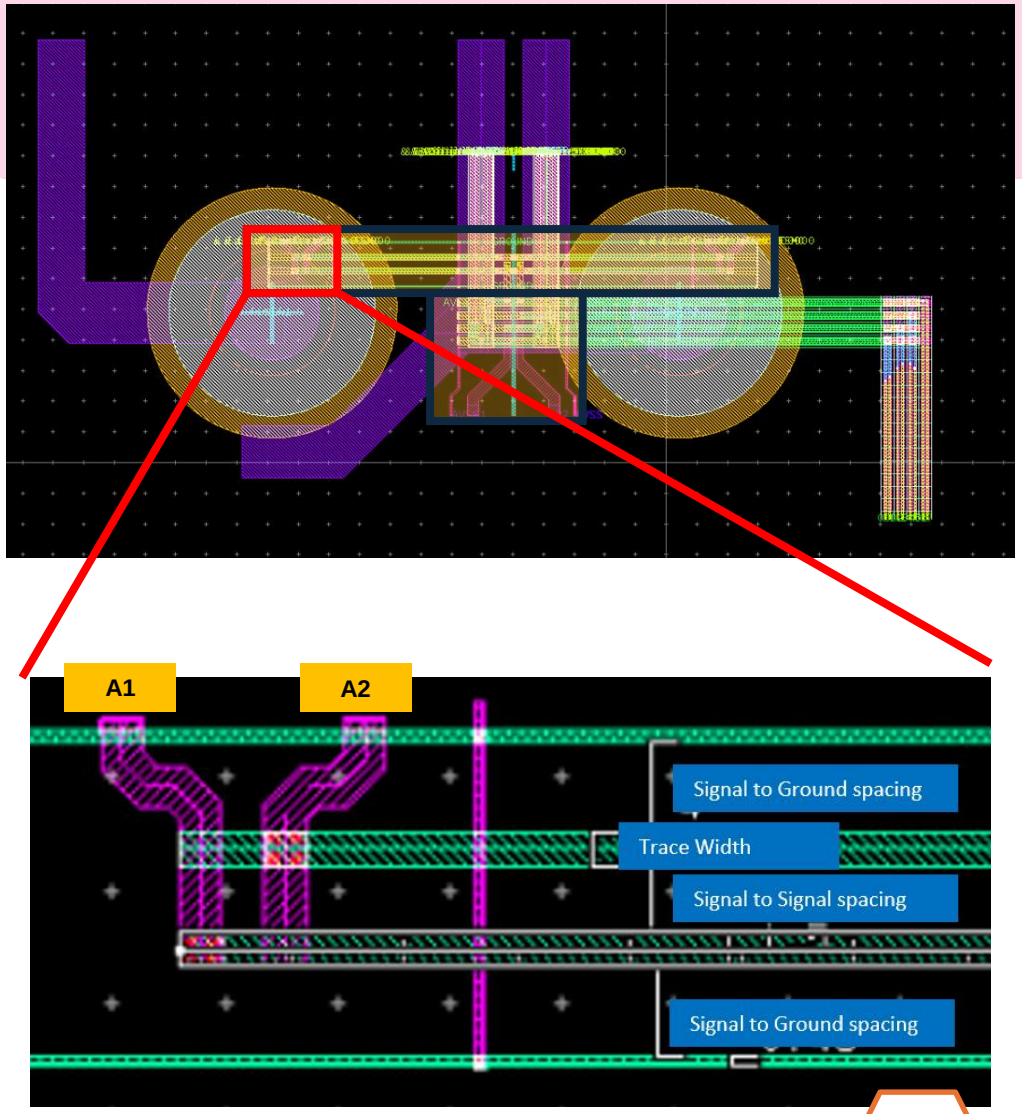
- Automates design of On-Chip Transmission Lines
- Trained metamodel useful for fast what-if analysis
- Finds optimal design based on desired circuit metrics
- All Extractions are using RaptorX EMag solver
- Easily build blocks from Bus-line Builder.
- Quickly build parameterized layout with readily available pyCells
  - Inductors
  - Baluns/Transformers
  - T-coils
  - Transmission Lines
  - Meets DRC rules
  - Consider layout dependent effect (LDE)





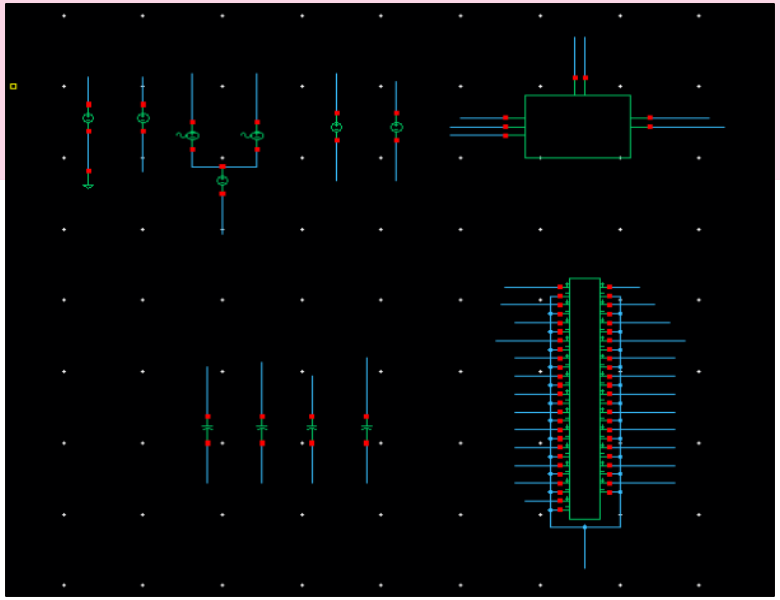
Start Design

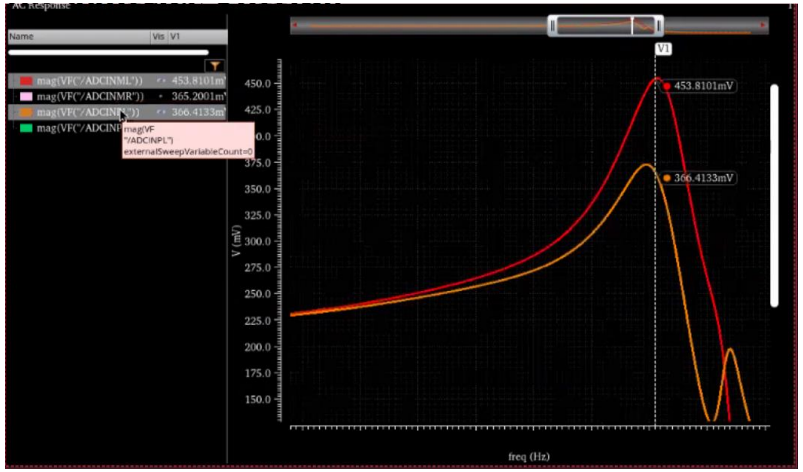
- Using advanced tech node process
- T-line main routed on topmost layers to minimize resistance
- Keep the T-line symmetrical structure
- Representative ground around T-line
- Output Pin location is fixed
- Bond-pad included in extraction
- Sweep:
  - Total trace length
  - Signal line width
  - Signal to Signal spacing
  - Signal to Ground spacing
  - Ground trace width



Circuit Metrics Setting

- Frequency response is using for optimization
- Testbench is running in Spectre
- Circuit metrics measured in Virtuoso platform
- Circuit metrics to optimize
  - Left side signal output pin peak voltage value.
  - Right side signal output pin peak voltage value.
  - Symmetrical metrics (Difference between left-side and right-side frequency response)

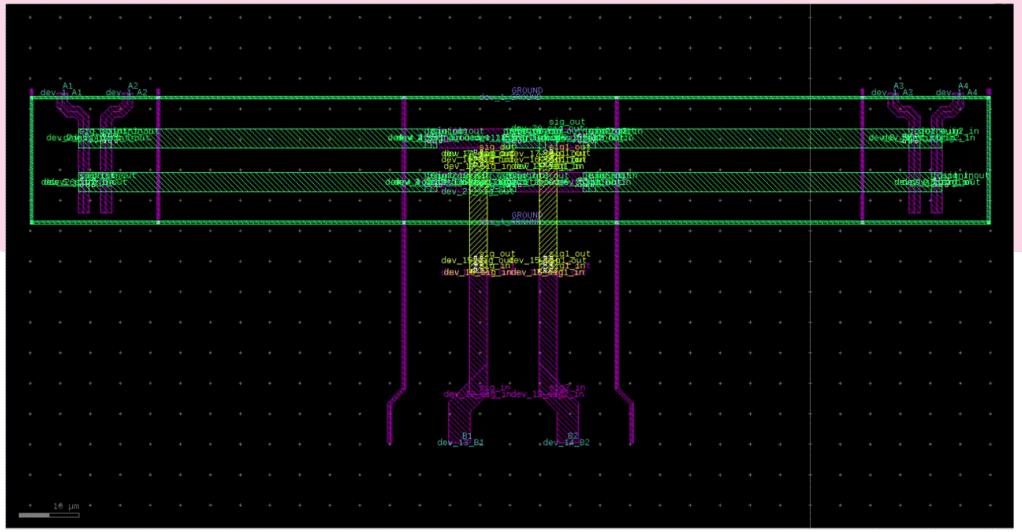


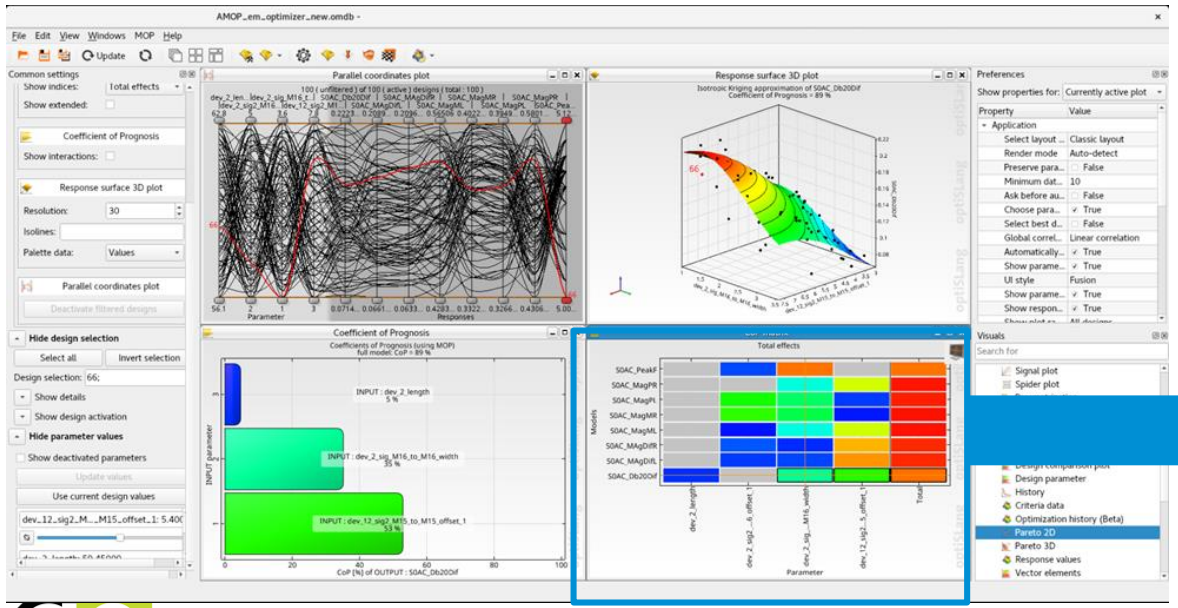


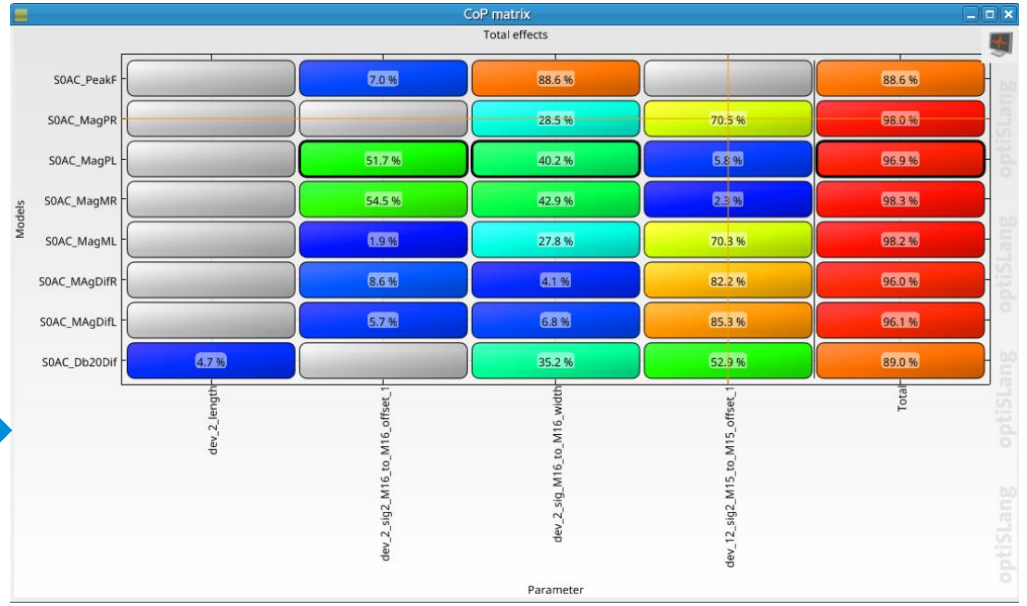
Name	Type	Details	Spec
S1AC_Ldb20	expr		
S1AC_Rdb20	expr		
S0AC_PeakF	expr		
S0AC_MagPR	expr		
S0AC_MagMR	expr		
S0AC_MagPL	expr		
S0AC_MagML	expr		
S0AC_MAgDifR	expr		< 20m
S0AC_MAgDifL	expr		< 20m
S0AC_Db20Dif	expr		< 0.05
S1AC_LMag	expr		
S1AC_RMag	expr		

Sensitivity Analysis

- Layout iterating 100 samples to train the Metamodel
- Sensitivity analysis analyze the coefficient of prognosis (CoP) between input and output

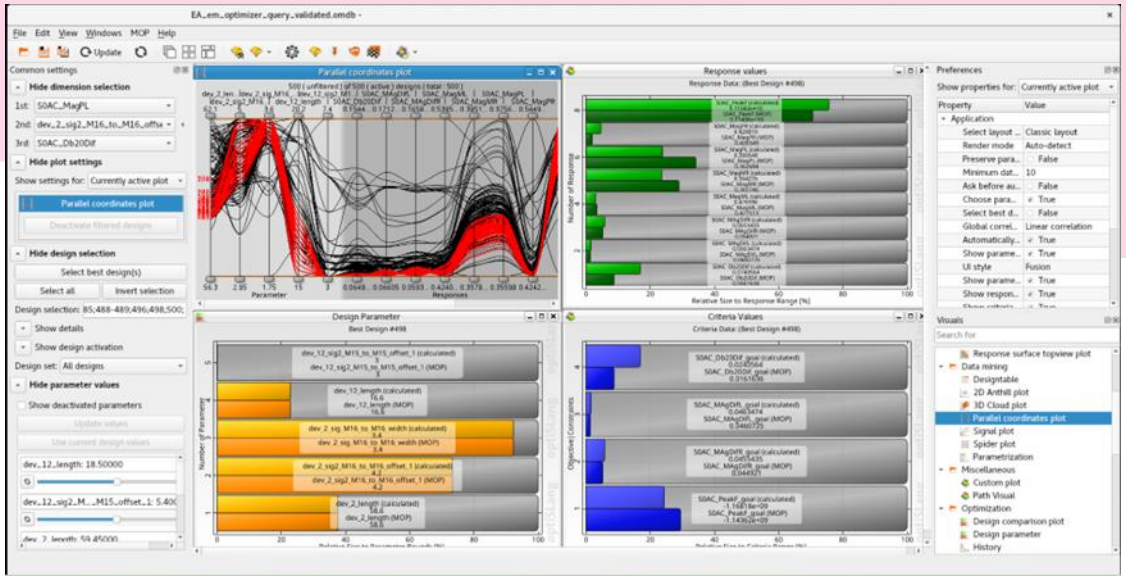


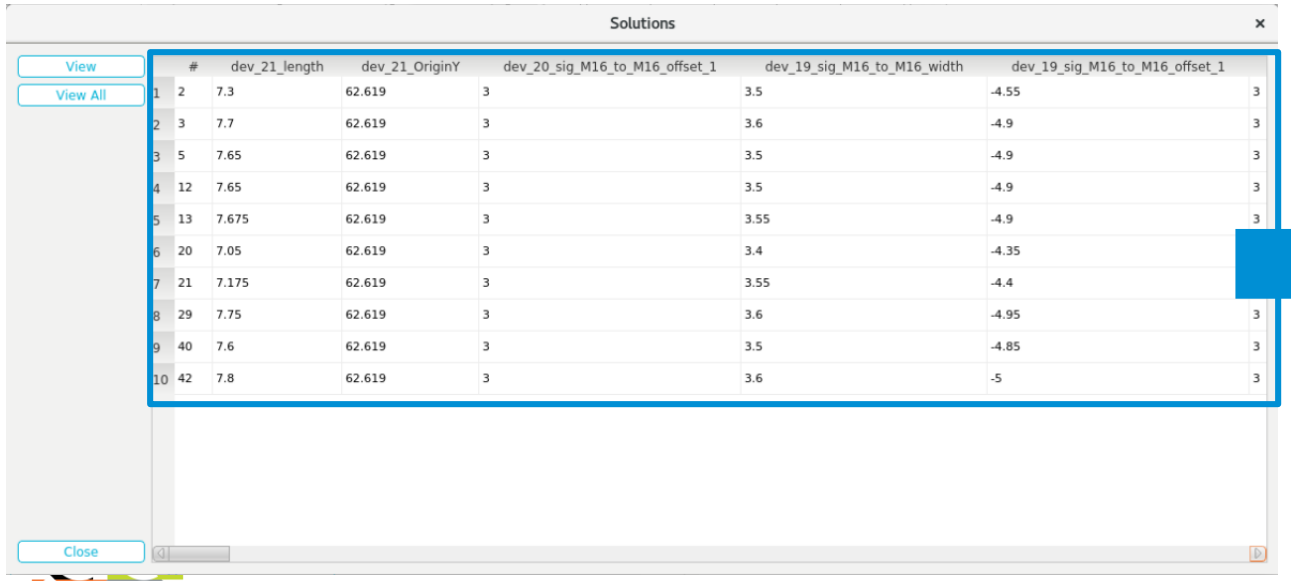




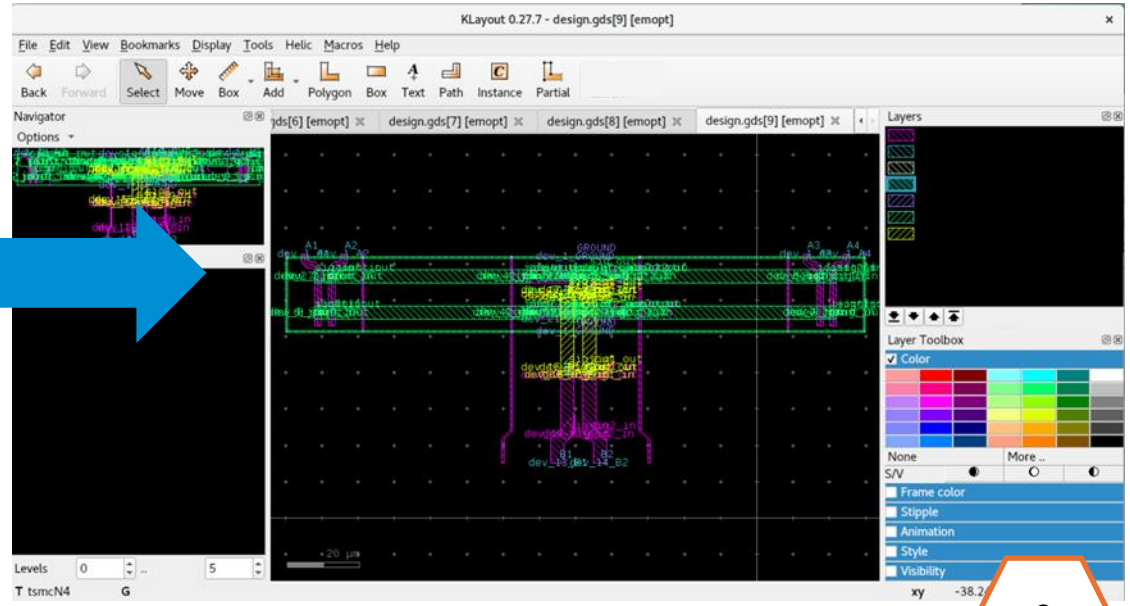
Optimization Result

- Use Metamodel predict the best possible solution
- Quickly explore which designs may hit minimum targets with parallel plots
- Call real solver to validate the predict best solution, and list the best candidate design





#	dev_21_length	dev_21_OriginY	dev_20_sig_M16_to_M16_offset_1	dev_19_sig_M16_to_M16_width	dev_19_sig_M16_to_M16_offset_1	
1	2	7.3	62.619	3	3.5	-4.55	3
2	3	7.7	62.619	3	3.6	-4.9	3
3	5	7.65	62.619	3	3.5	-4.9	3
4	12	7.65	62.619	3	3.5	-4.9	3
5	13	7.675	62.619	3	3.55	-4.9	3
6	20	7.05	62.619	3	3.4	-4.35	3
7	21	7.175	62.619	3	3.55	-4.4	3
8	29	7.75	62.619	3	3.6	-4.95	3
9	40	7.6	62.619	3	3.5	-4.85	3
10	42	7.8	62.619	3	3.6	-5	3



Optimization Result

Results Table before and after optimization				
Designs	AC_MAGdiff_R (mV)	AC_MAGdiff_L (mV)	AC_MAGdiff_L&R (dB)	Iteration Time
spec	<20mV	<20mV	<0.05dB	
Initial Layout	96.04	96.12	0.0834	Weeks
AI Optimized Layout	44.78	45.62	0.0274	1hr

- AI Optimized Layout:
  - Improved AC performance by over 50%
  - Improved symmetrical metrics from 0.0834 dB to 0.0274 dB
  - Cut iteration time from **weeks to just 1 hour**

Conclusion

- **This work proposes an AI-driven, EM-aware optimization flow for efficient on-die transmission line design.**
  - In high-speed SerDes design, transmission line modeling simulation is required to minimizing the associated signal processing risks, especially in high-speed clock simulation analysis.
  - Adopting AI-driven ML based MOP methods for transmission line design enables automatic multi-parameters, multi-objectives optimization. With the approach, we can efficiently obtain multiple designs that meet target values and dramatically reduce the layout iterations ranging from weeks to hours.
  - Through this flow improvement, we make transmission line layout optimization easy and efficient, significantly improve design efficiency.